

MS7004V10A

TITLE	SHEET
COVER SHEET	1
BLOCK DIAGRAM	2
PWR MAP/CLOCK MAP	3
GPIO/MEMORY/PCI/HW STRPPING	4
PROCESSOR (SOCKET478)	5, 6
NORTH BRIDGE PM800/PT800CE	7 -- 10
DIMM1 / DIMM2	11
DDR TERMINATIONS	12
AGP SLOT	13
SOUTH BRIDGE VT8237/VT8235CE	14 -- 16
PCI SLOTS 1-3	17
AC'97 AUDIO	18
LAN	19
IDE CONNECTORS & CNR	20
USB CONNECTORS	21
LPC SUPER IO & FLOPPY CONNECTOR	22
PARALLEL / SERIAL / VGA	23
ATX POWER CONNECTOR / FRONT PANEL	24
CLOCK GEN.	25
MS7 ACPI CONTROLLER	26
VRM10.0(FMB1)	27
EMI & MISC.	28
HISTORY	29

CPU:

Intel Northwood/Prescott
Up to 3.6GHz

System Chipset:

PM800/PT800 (North Bridge)
VIA 8237 (South Bridge)

On Board Chipset:

BIOS -- ISA EEPROM
AC'97 Codec --ALC655
LPC Super I/O -- W83697HF
LAN -- PHY RTL8201
CLOCK -- CY28341-3

Main Memory:

DDR * 2 (Max 2GB)

Expansion Slots:

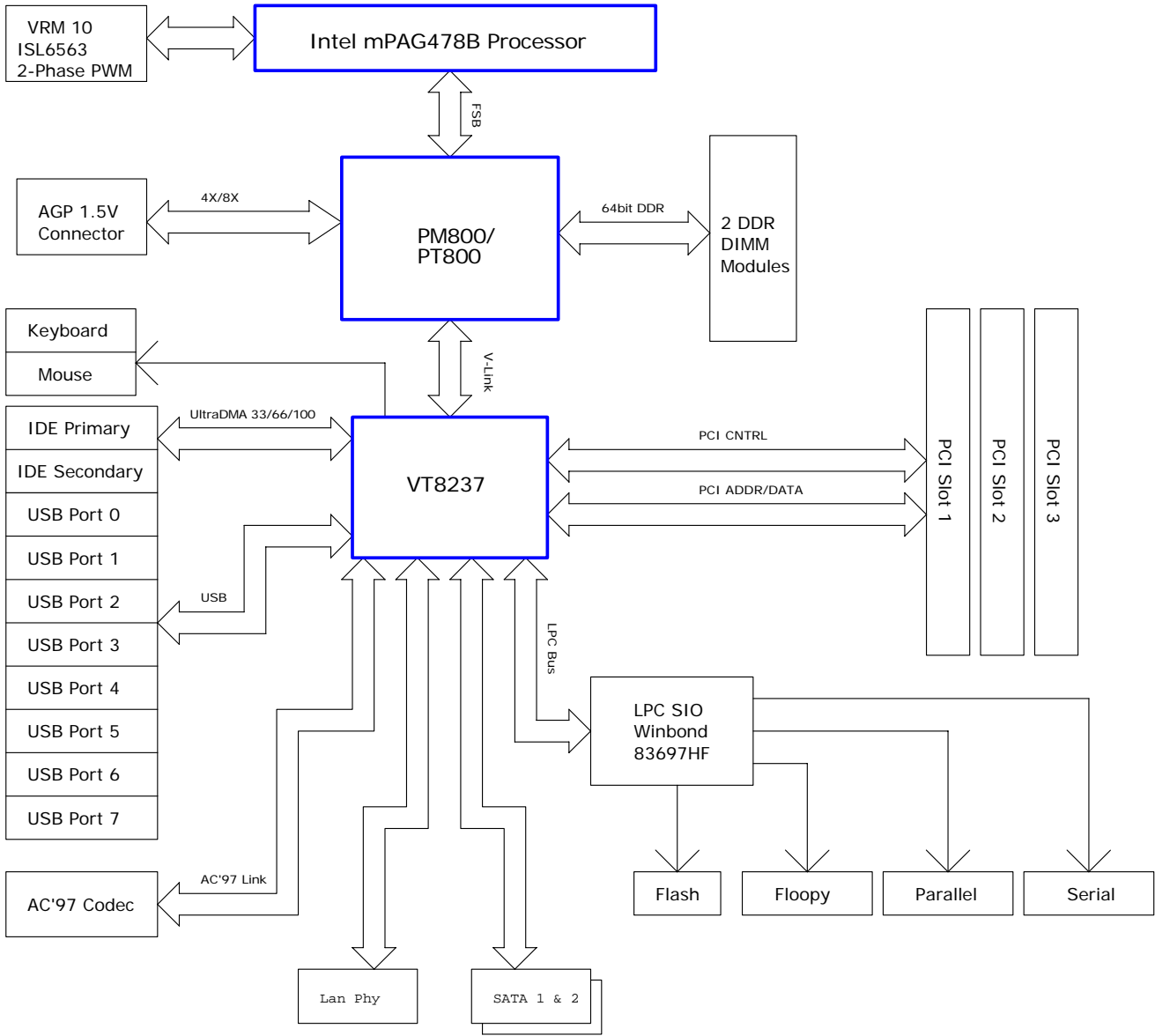
AGP * 1
PCI2.3 SLOT * 3
CNR * 1

PWM:

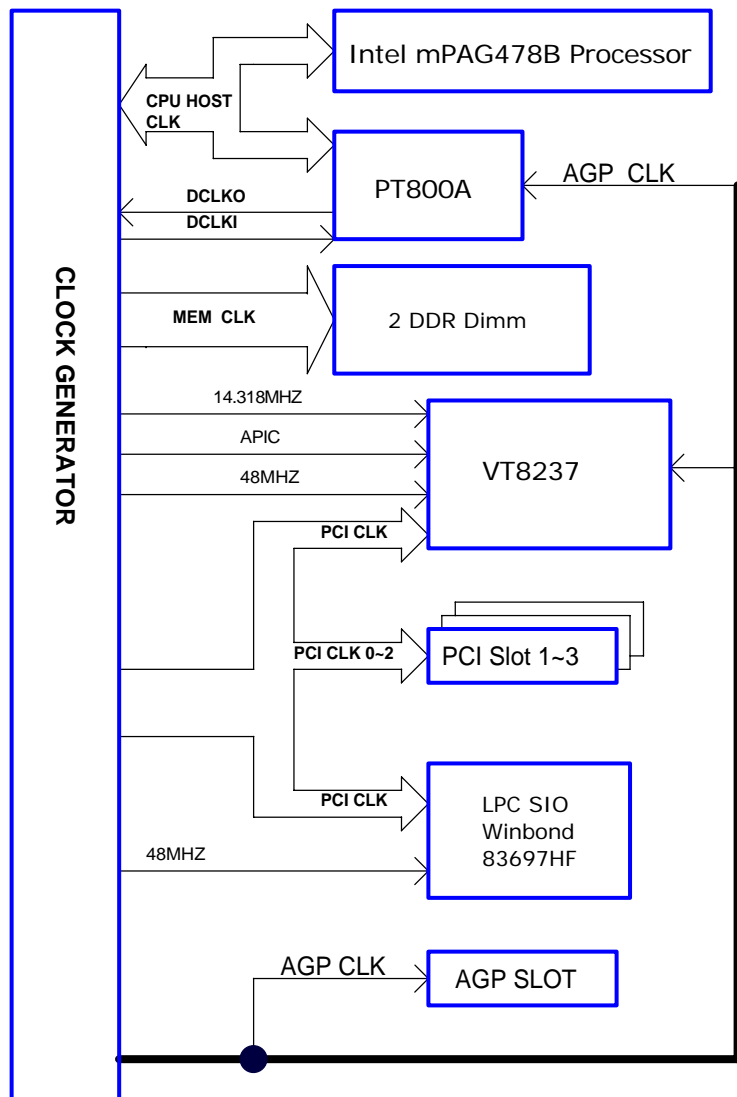
Controller: STL6710

Micro-Star			
Title			
COVER SHEET			
Size	Document Number		Rev
	MS-7004		10A
Date:	Wednesday, February 25, 2004	Sheet	1 of 29

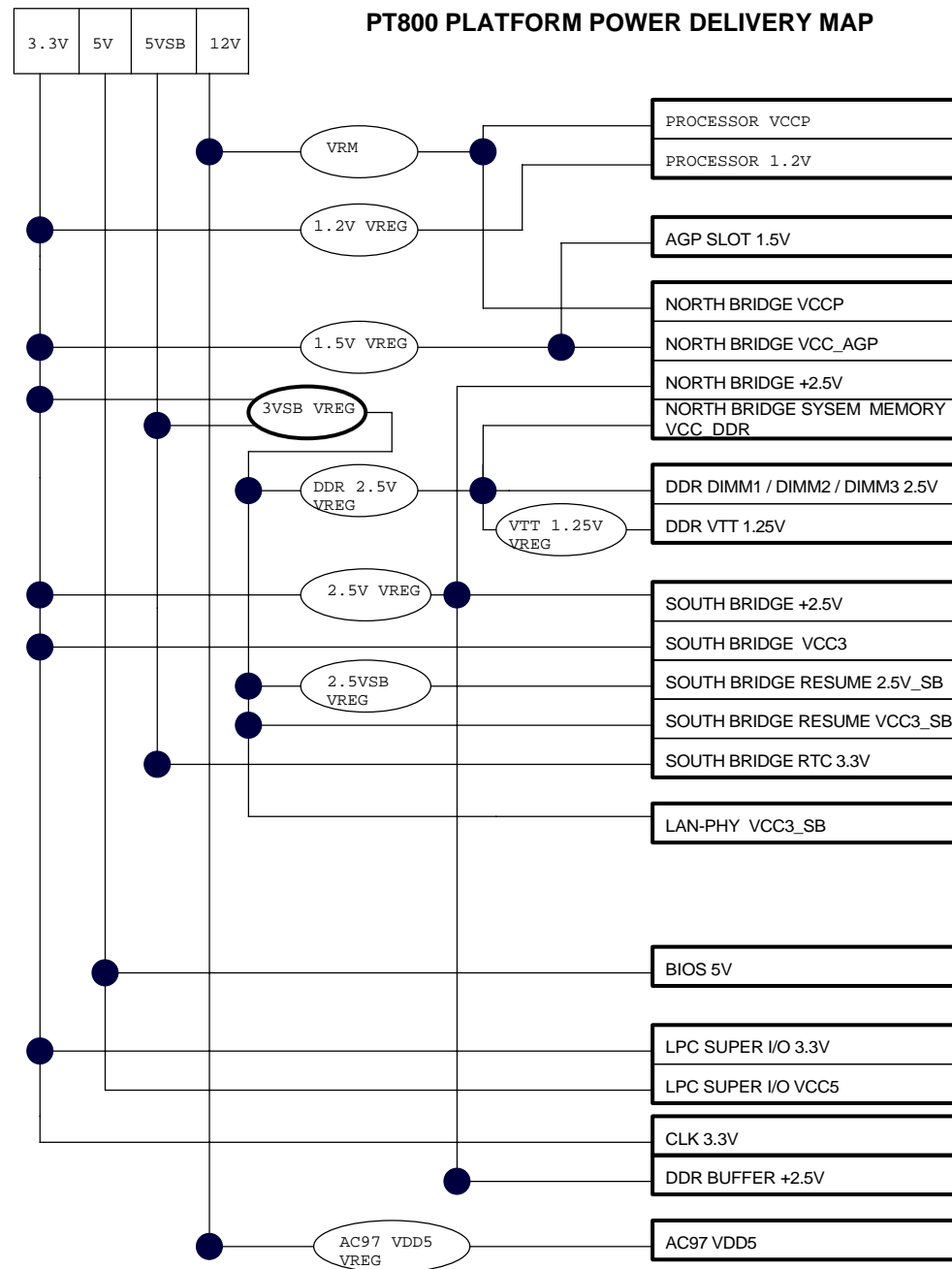
Block Diagram



PT800 PLATFORM CLOCK GENERATOR MAP



PT800 PLATFORM POWER DELIVERY MAP



Micro-Star

Title			
PWR AND CLOCK MAP			
Size	Document Number		Rev
	MS-7004		10A
Date:	Wednesday, February 25, 2004	Sheet	3 of 29
	2		1

NB

GPIO Pin	Type	Function	Power well
GPI 0	I	GPI 0	RESUME
GPI 1	I	IDE2 CBD	RESUME
GPO 0	I	GPO 0	RESUME
GPO 1	I	GPO 0	RESUME
GPIO A	I	NB STR S	MAIN
GPIO B	I	IOQ DEPH	MAIN
GPIO C	I	NB STR S	MAIN
GPIO D	I	GTL PULL	MAIN

I/O

GPIO 10	I/O	HI	MAIN
GPIO 11	I/O	HI	MAIN
GPIO 12	I/O	HI	MAIN
GPIO 13	I/O	NA	MAIN
GPIO 14	I/O	NA	MAIN
GPIO 15	I/O	NA	MAIN
GPIO 16	I/O	NA	MAIN
GPIO 17	I/O	NA	MAIN
GPIO 18	I/O	NA	MAIN
GPIO 19	I/O	NA	MAIN
GPIO 20	I/O	NA	MAIN
GPIO 21	I/O	NA	MAIN
GPIO 22	I/O	NA	MAIN

default output
default output
default output

PCI Config.

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK	CLK GEN PIN OUT
PCI Slot 1	INTA# INTB# INTC# INTD#	PCI_REQ#0 PCI_GNT#0	AD19	PCICLK0	18 (PCI_CLK0)
PCI Slot 2	INTB# INTC# INTD# INTA#	PCI_REQ#1 PCI_GNT#1	AD20	PCICLK1	19 (PCI_CLK1)
PCI Slot 3	INTC# INTD# INTA# INTB#	PCI_REQ#2 PCI_GNT#2	AD21	PCICLK2	21 (PCI_CLK2)
PCI Slot 4	INTD# INTA# INTB# INTC#	PCI_REQ#3 PCI_GNT#3	AD22	PCICLK3	14 (PCI_CLK3)
PCI Slot 5	INTA# INTB# INTC# INTD#	PCI_REQ#4 PCI_GNT#4	AD23	PCICLK4	17 (PCI_CLK4)

FWH

GPIO Pin	Type	Function
GPI 0	I	Pull UP through 1K ohms (unused)
GPI 1	I	Pull UP through 1K ohms (unused)
GPI 2	I	Pull UP through 1K ohms (unused)
GPI 3	I	Pull UP through 1K ohms (unused)
GPI 4	I	Pull UP through 1K ohms (unused)

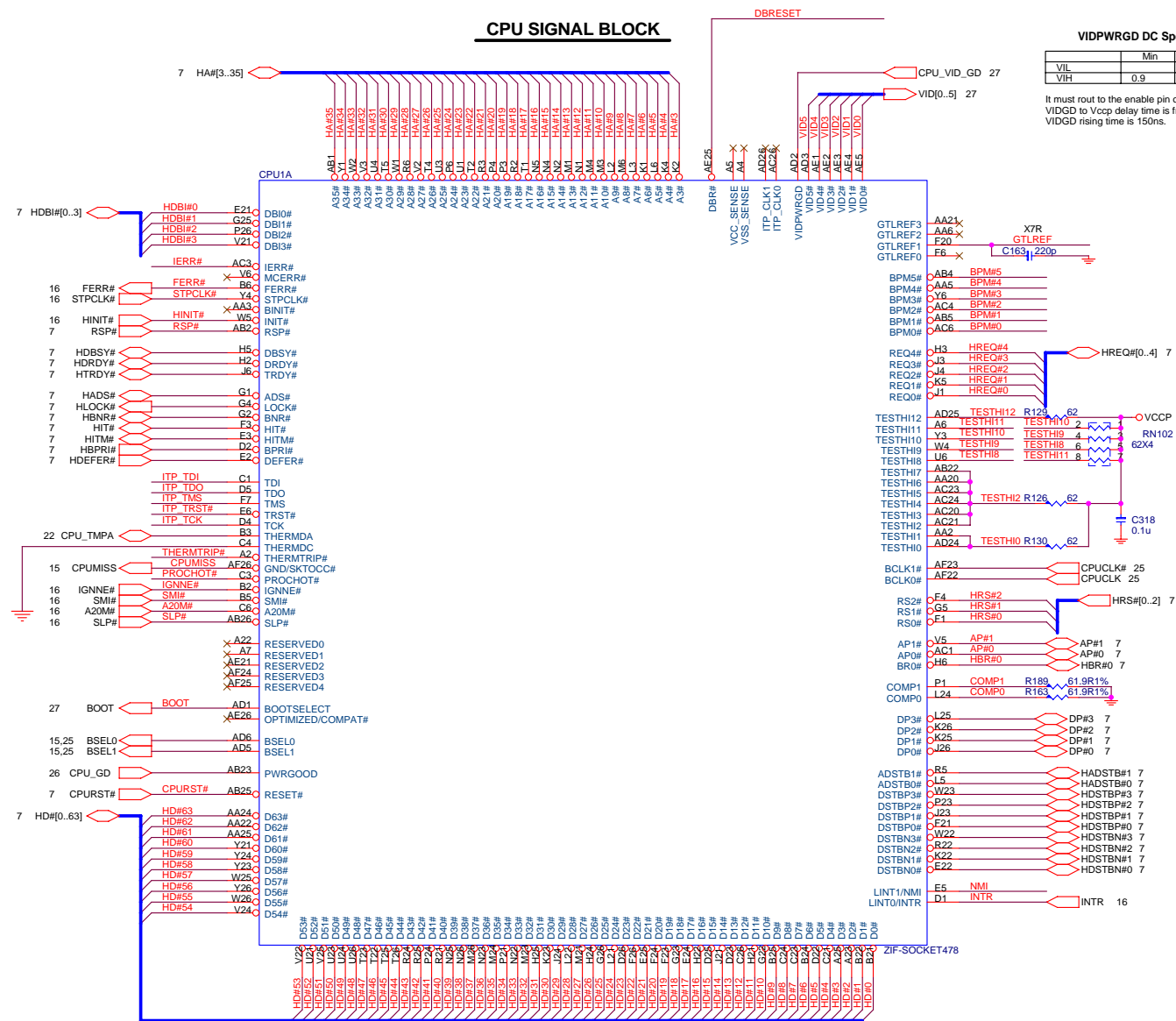
DDR DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	1010000B	MCLK0/MCLK#0 MCLK1/MCLK#1 MCLK2/MCLK#2
DIMM 2	1010001B	MCLK3/MCLK#3 MCLK4/MCLK#4 MCLK5/MCLK#5
DIMM 3	1010010B	MCLK6/MCLK#6 MCLK7/MCLK#7 MCLK8/MCLK#8

PCI RESET DEVICE

Signals	Target
PCIRST#1	SB, NB
PCIRST#2	PCI slot 1-3, 1394, FWH
HD_RST#	Primary, Scondary IDE

CPU SIGNAL BLOCK

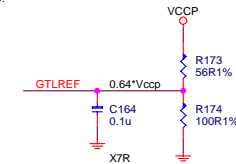


VIDPWRGD DC Specifications

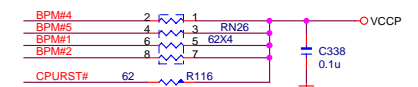
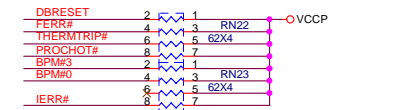
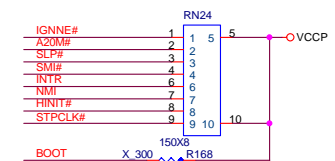
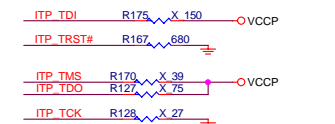
	Min	Typ	Max
VIL			0.3
VIH	0.9		

It must route to the enable pin of PWM and CK-409.
VIDGD to Vccp delay time is from 1ms to 10ms.
VIDGD rising time is 150ns.

CPU GTL REFERENCE VOLTAGE BLOCK



CPU ITP BLOCK

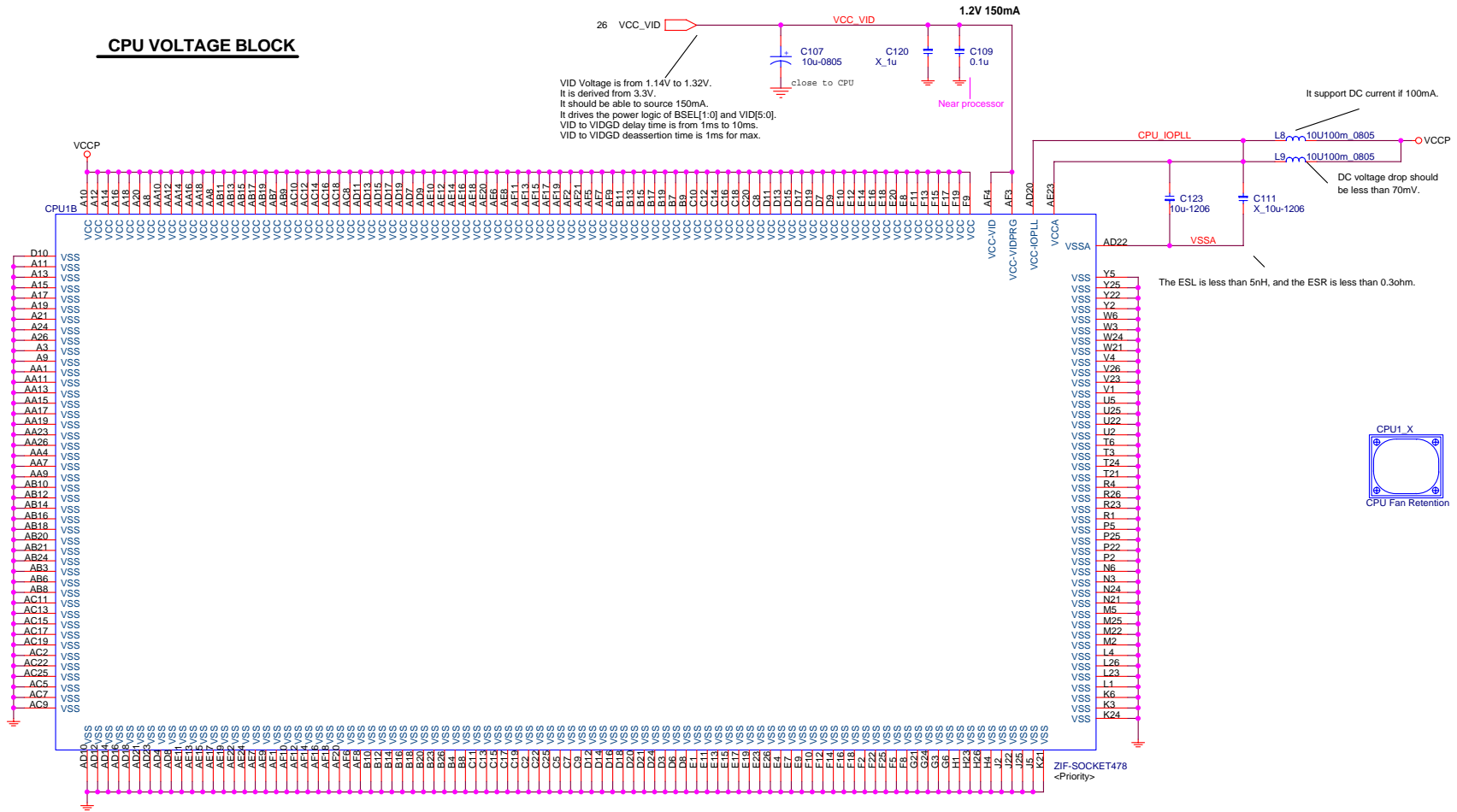


CPU STRAPPING RESISTORS

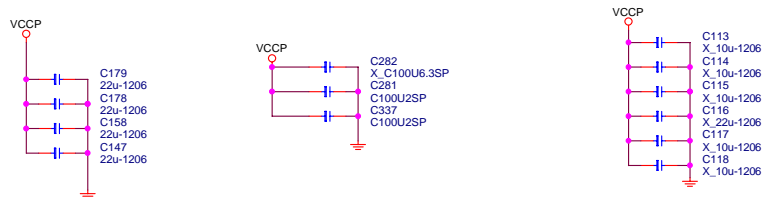
ALL COMPONENTS CLOSE TO CPU



CPU VOLTAGE BLOCK



CPU DECOUPLING CAPACITORS

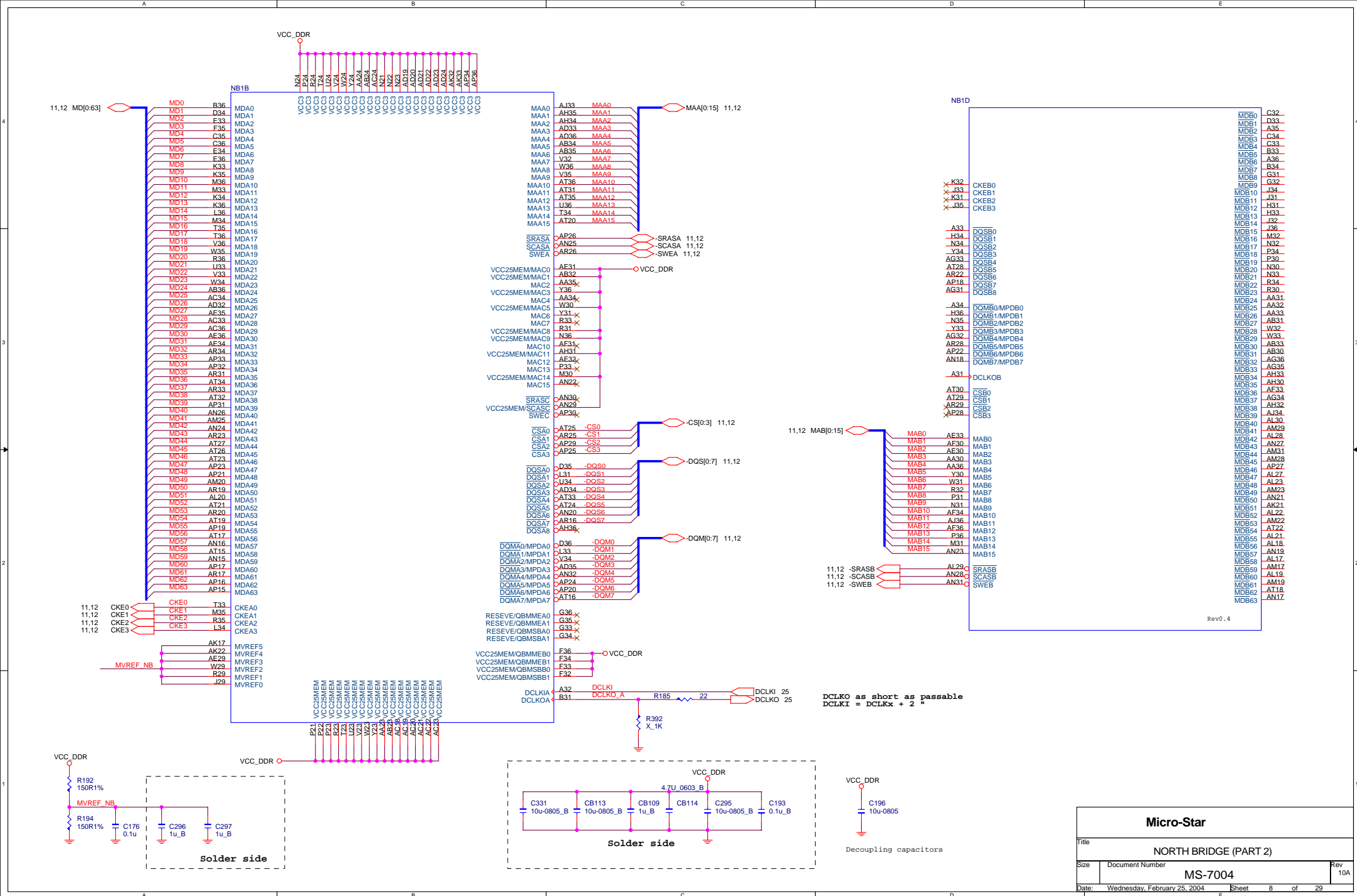


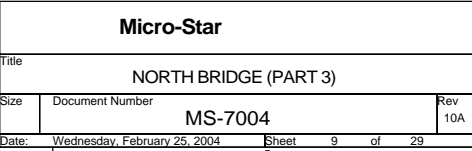
Micro-Star

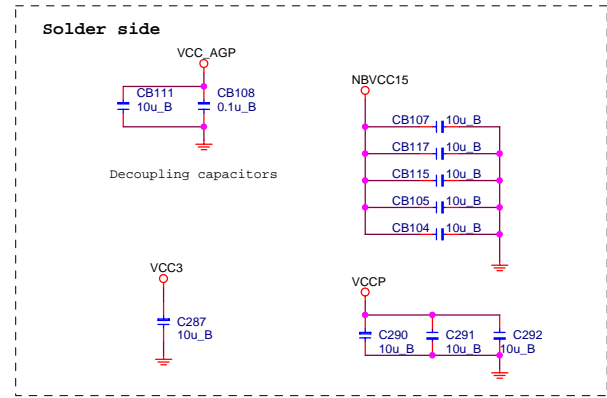
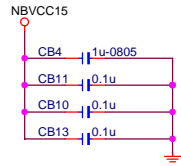
Title Intel mPGA478B - Power

Size Document Number MS-7004 Rev 10A

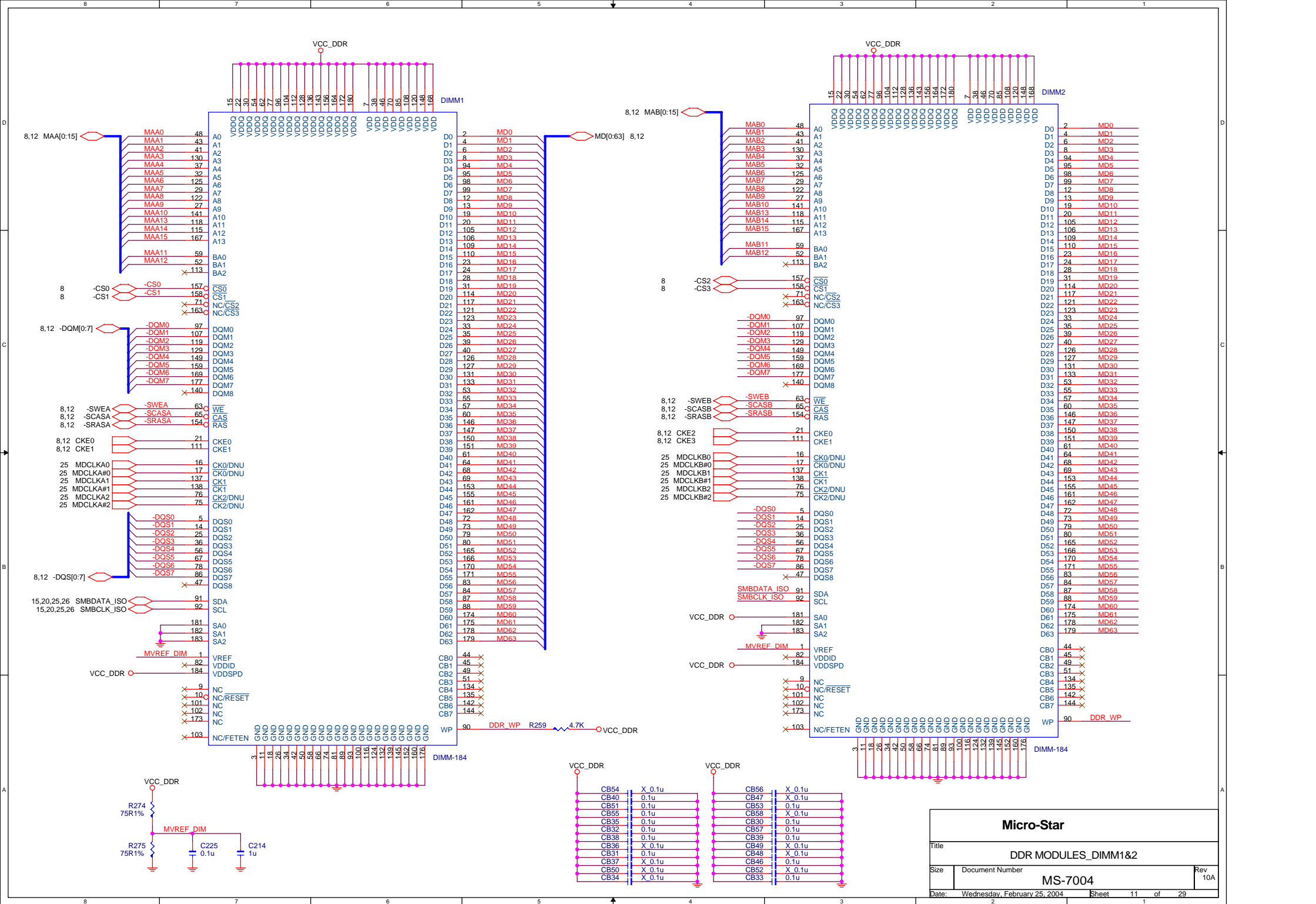
Date: Wednesday, February 25, 2004 Sheet 6 of 29







Micro-Star			
Title			
NORTH BRIDGE (PART4)			
Size	Document Number		Rev
	MS-7004		10A
Date:	Wednesday, February 25, 2004		Sheet 10 of 29



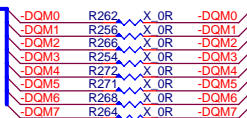
8,11 MD[0:63] MD[0:63] MD[0:63] 8,11



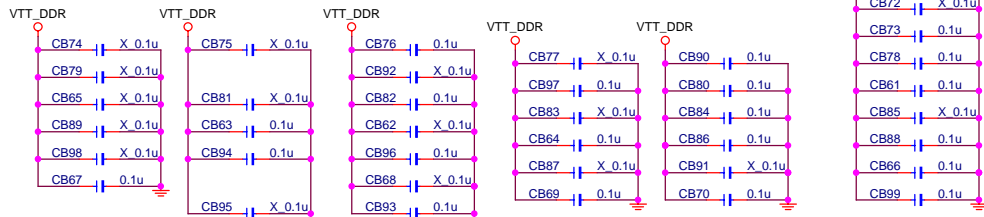
8,11 -DQS[0:7] -DQS[0:7] -DQS[0:7] 8,11



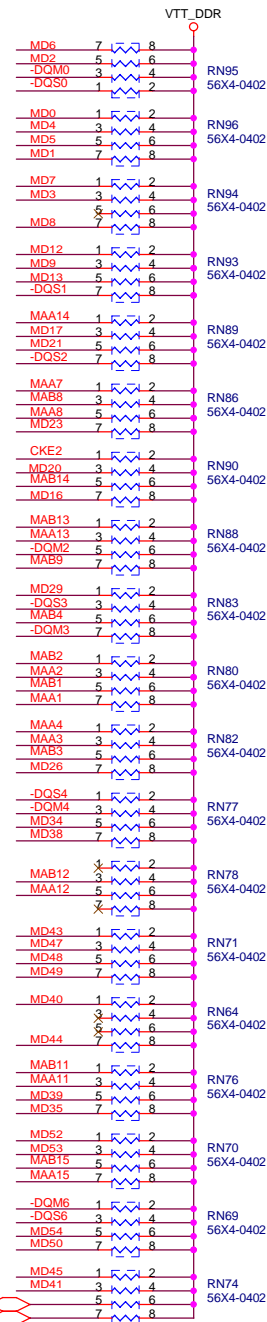
8,11 -DQM[0:7] -DQM[0:7] -DQM[0:7] 8,11



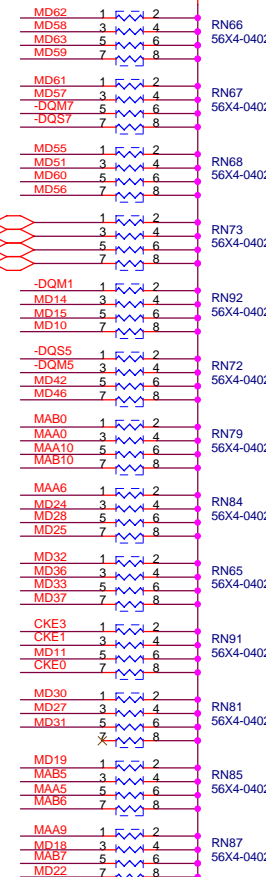
VTT_DDR



8,11 -SCASB
8 -CS2

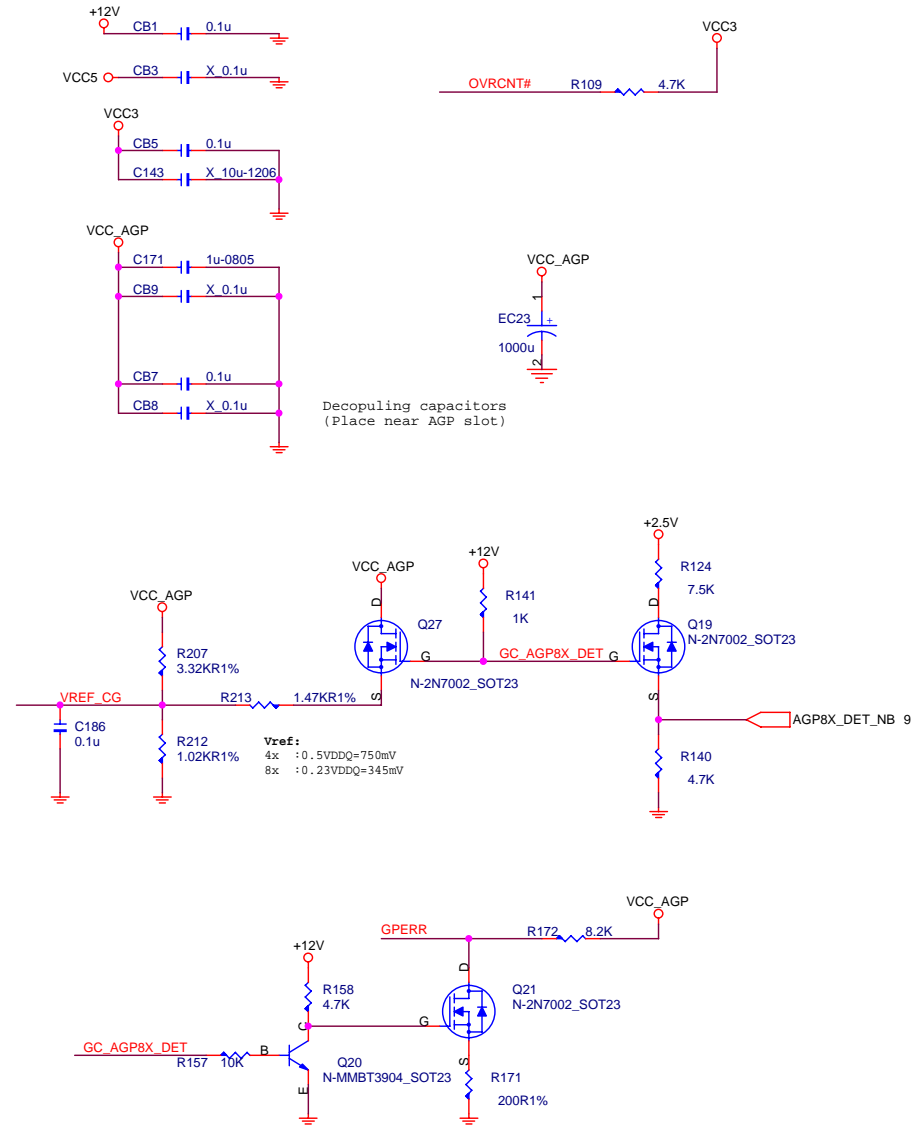
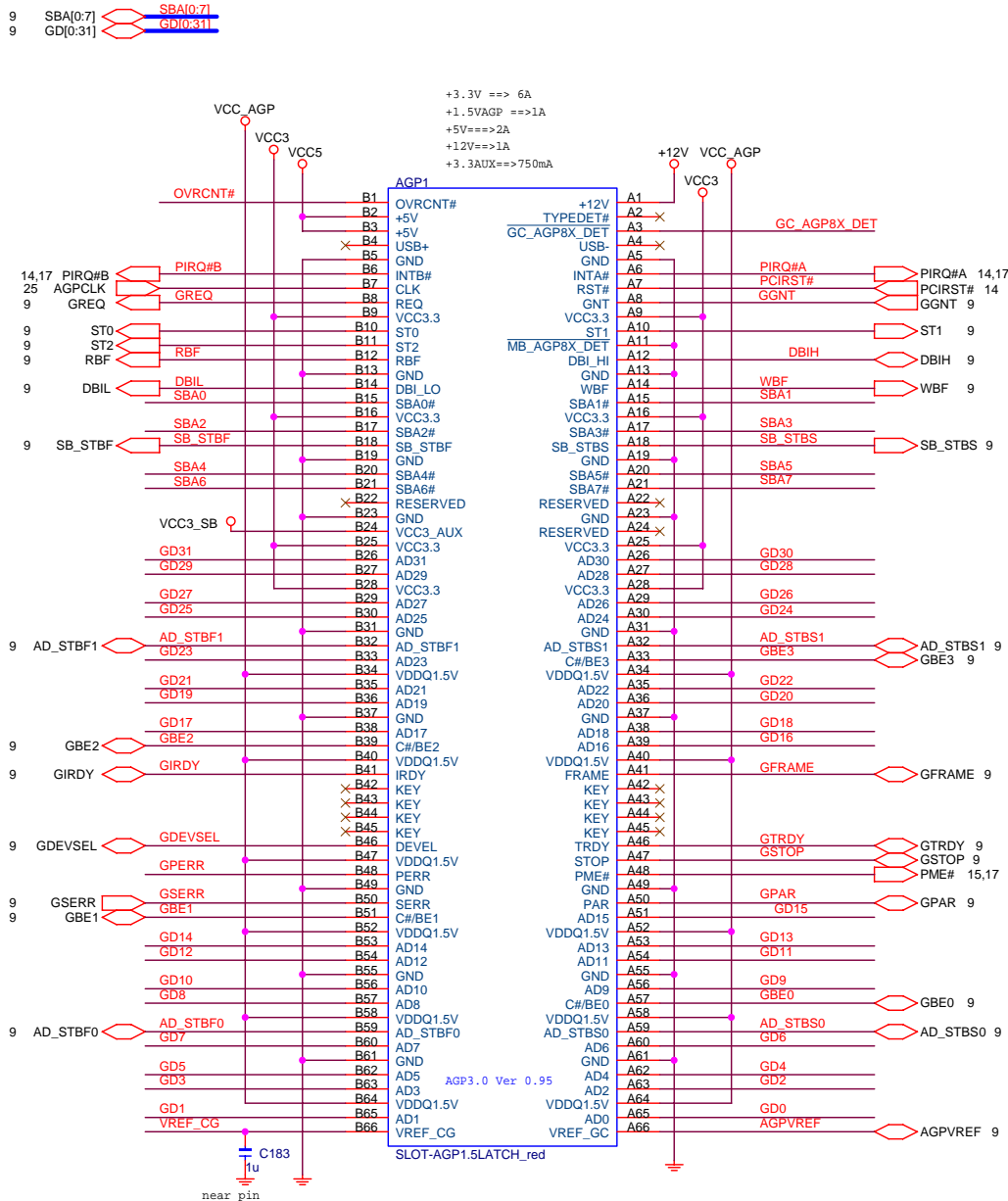


VTT_DDR



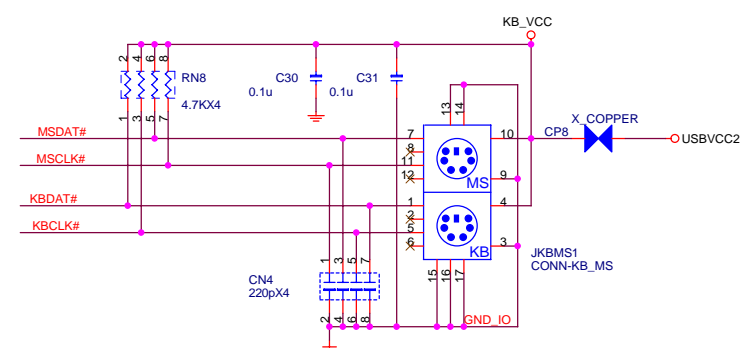
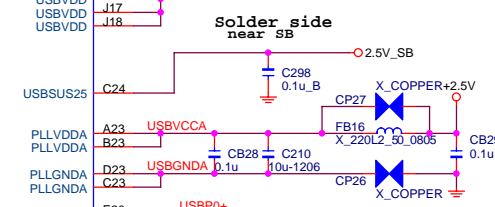
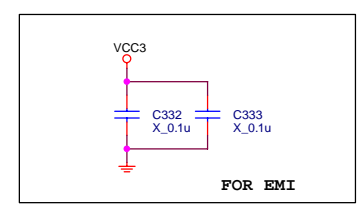
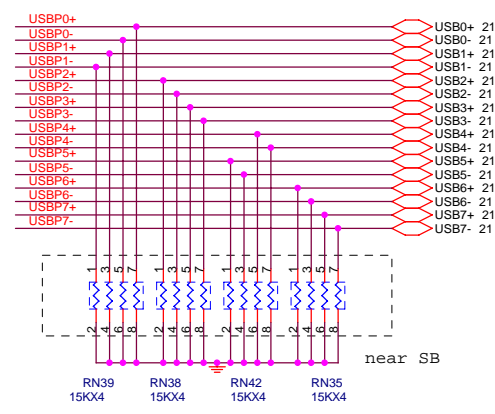
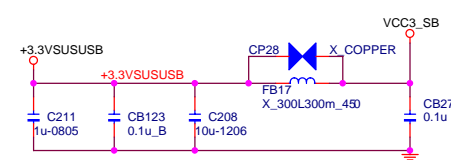
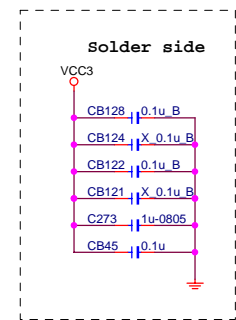
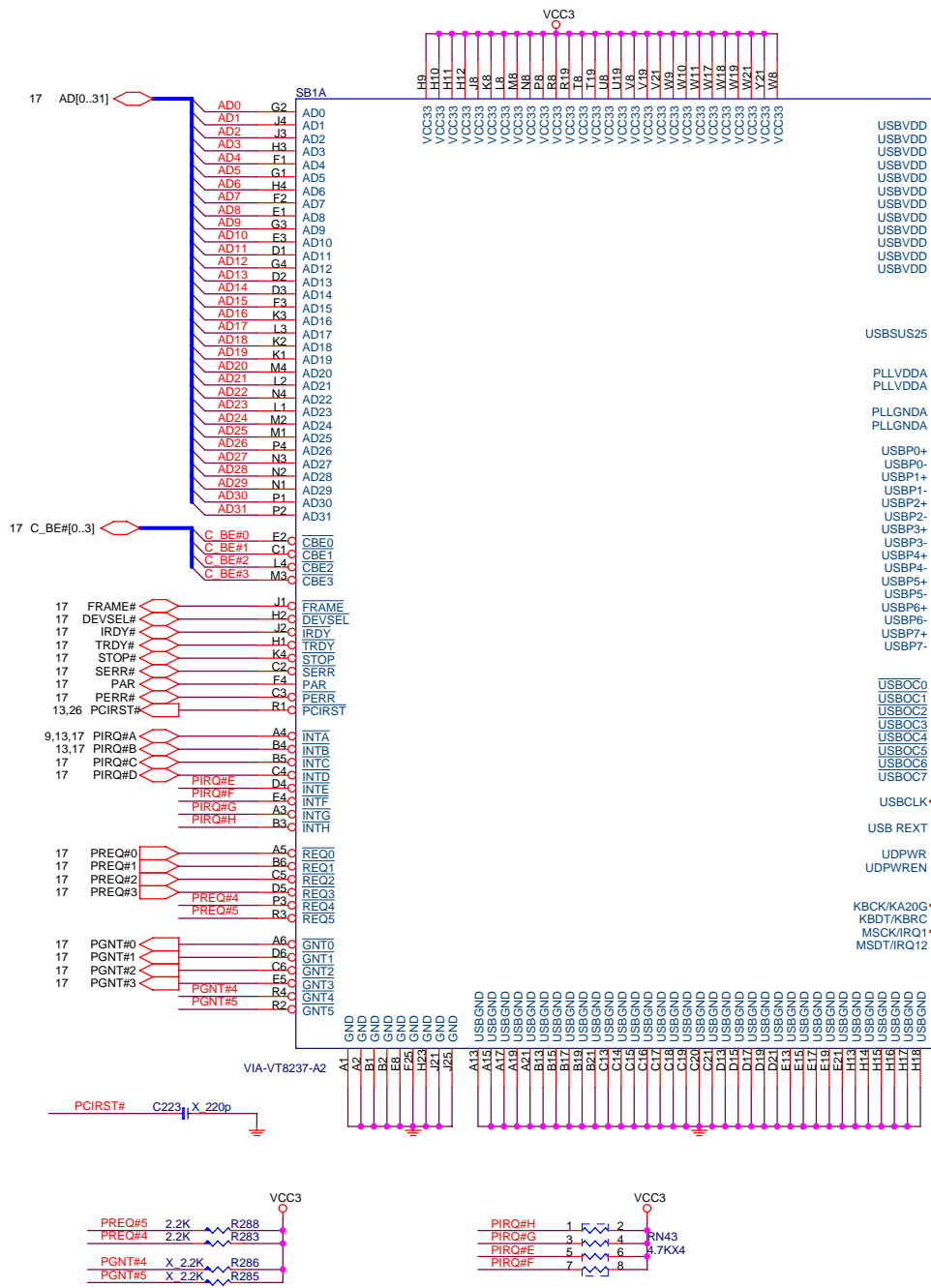
8,11 MAA[0:15]
8,11 MAB[0:15]
8,11 CKE[0:3]

Micro-Star			
Title			
DDR TERMINALS			
Size	Document Number	Rev	
		MS-7004	
Date:	Wednesday, February 25, 2004	Sheet	12 of 29
		E	

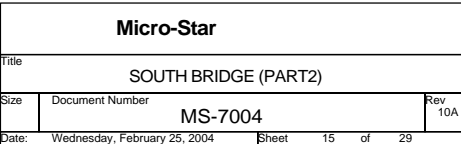


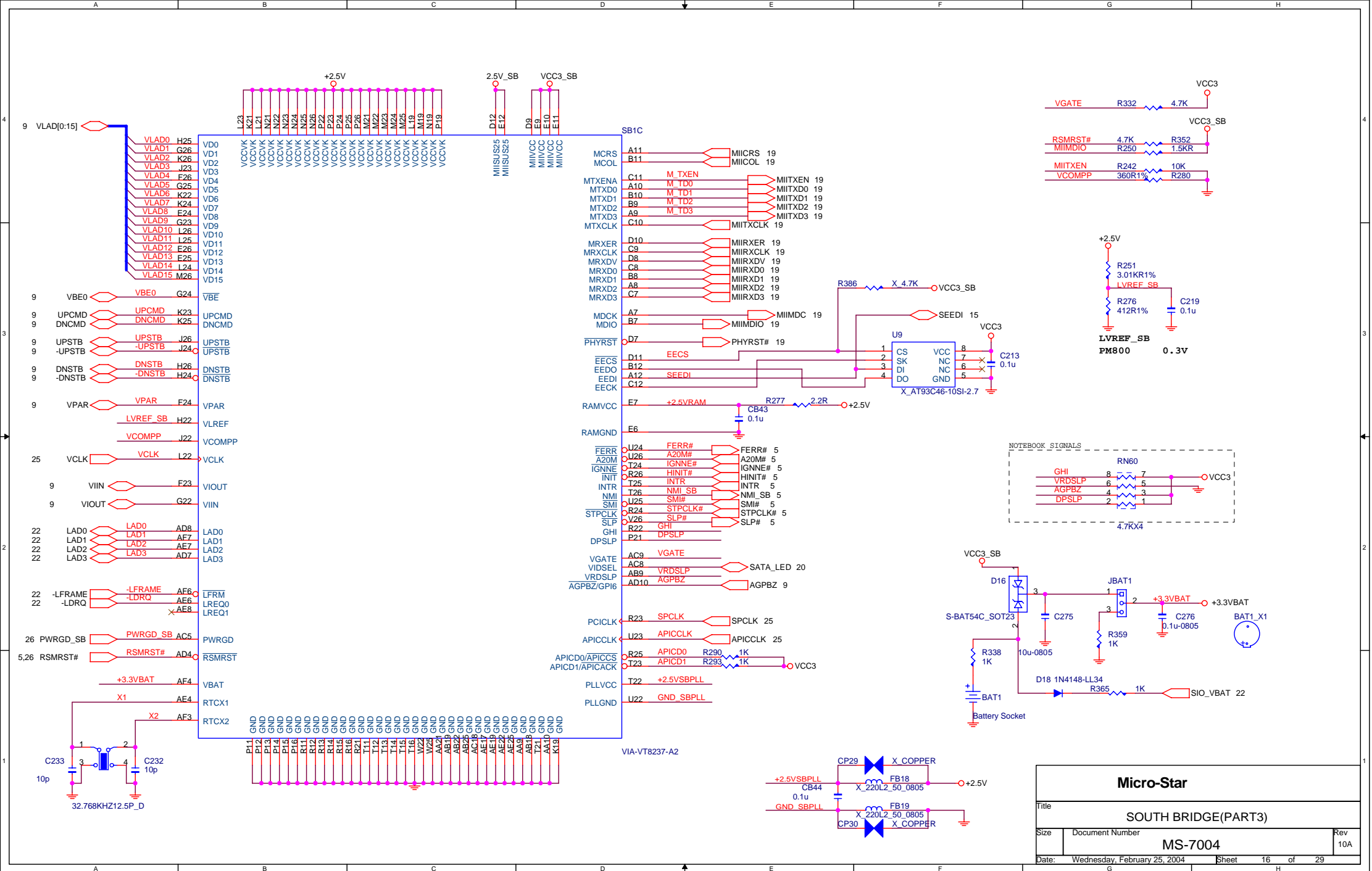
Micro-Star

Title			AGPSLOT	
Size	Document Number		MS-7004	
Date:	Wednesday, February 25, 2004		Sheet	13 of 29

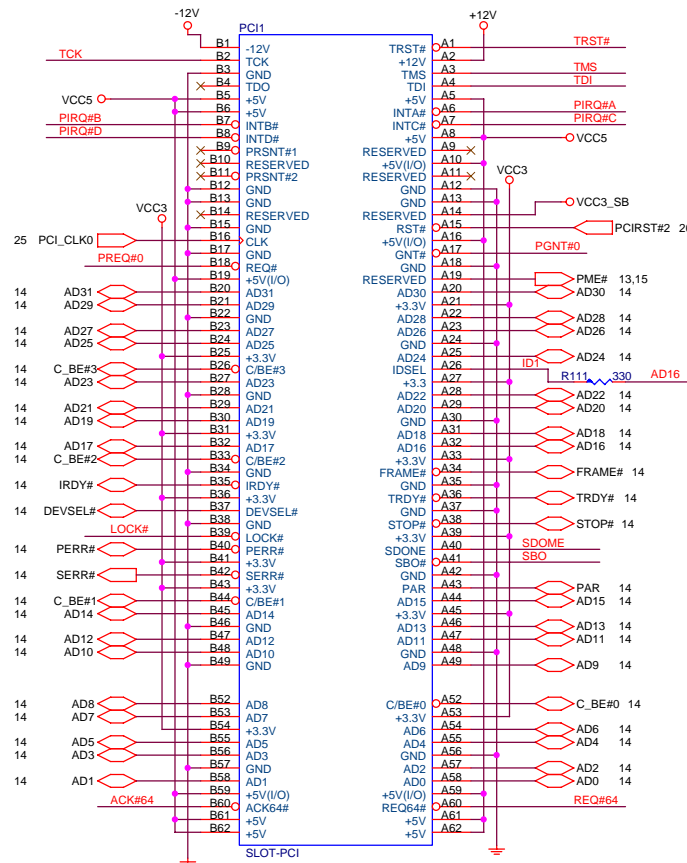


Micro-Star			
Title			
SOUTH BRIDGE (PART1)			
Size	Document Number	Rev	
	MS-7004	10A	
Date:	Wednesday, February 25, 2004	Sheet	14 of 29



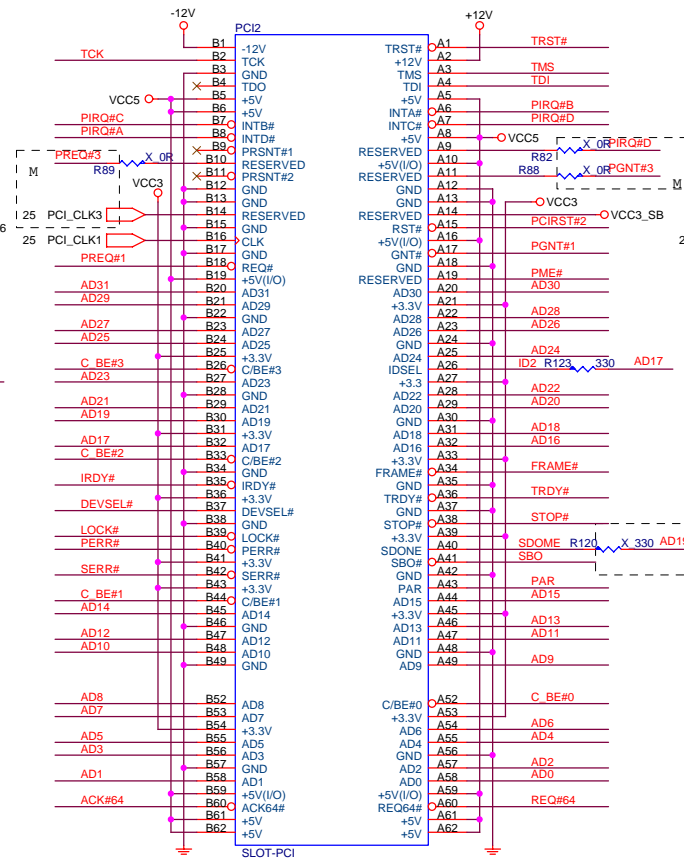


PCI SLOT 1 (PCI VER: 2.2 COMPLY)



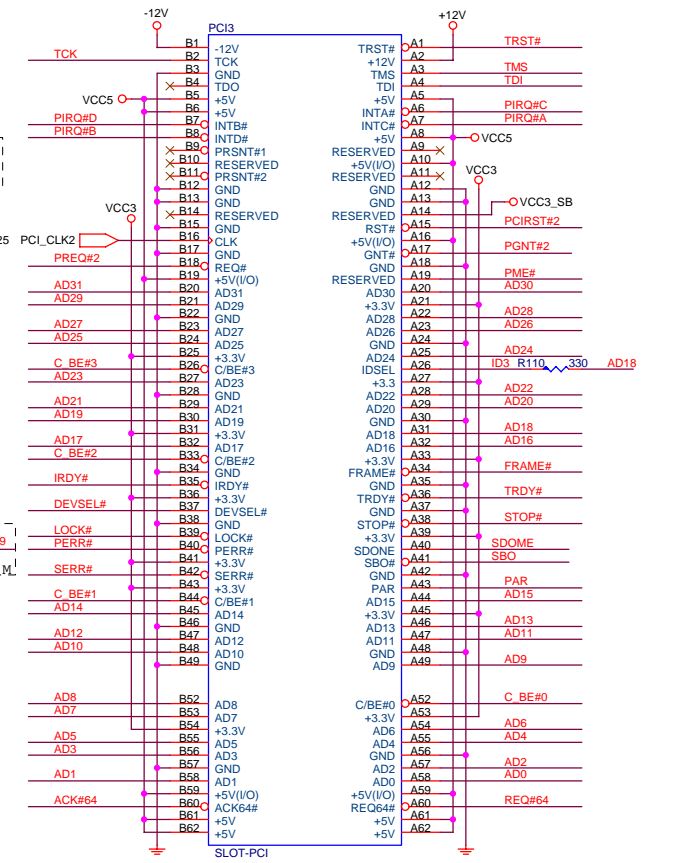
AD16, PREQ#0, PIRQ#A

PCI SLOT 2 (PCI VER: 2.2 COMPLY)



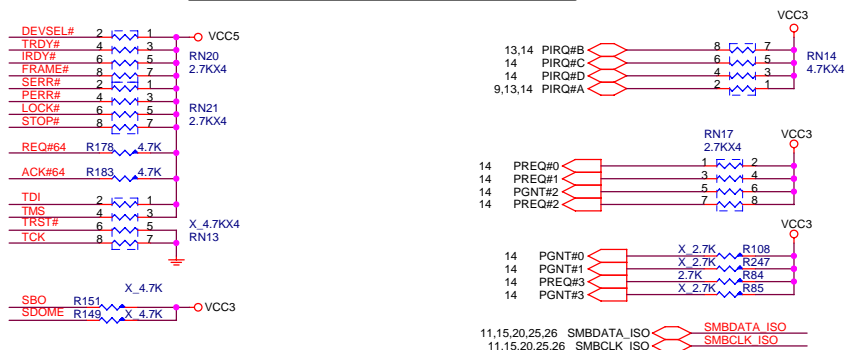
AD17, PREQ#1, PIRQ#B
AD19, PREQ#3, PIRQ#D

PCI SLOT 3 (PCI VER: 2.2 COMPLY)

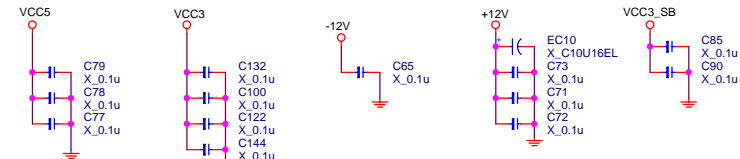


AD18, PREQ#2, PIRQ#C

PCI PULL-UP / DOWN RESISTORS



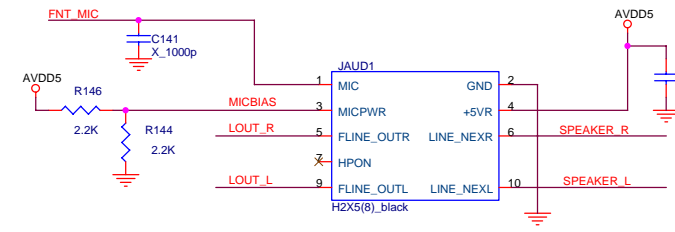
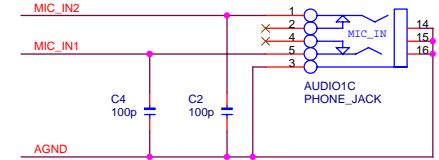
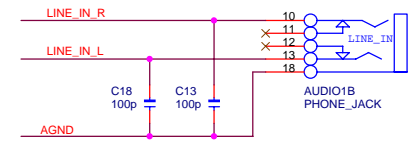
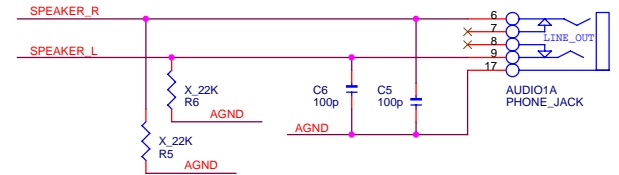
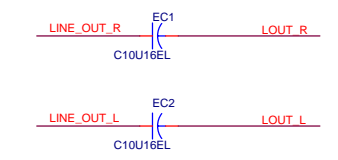
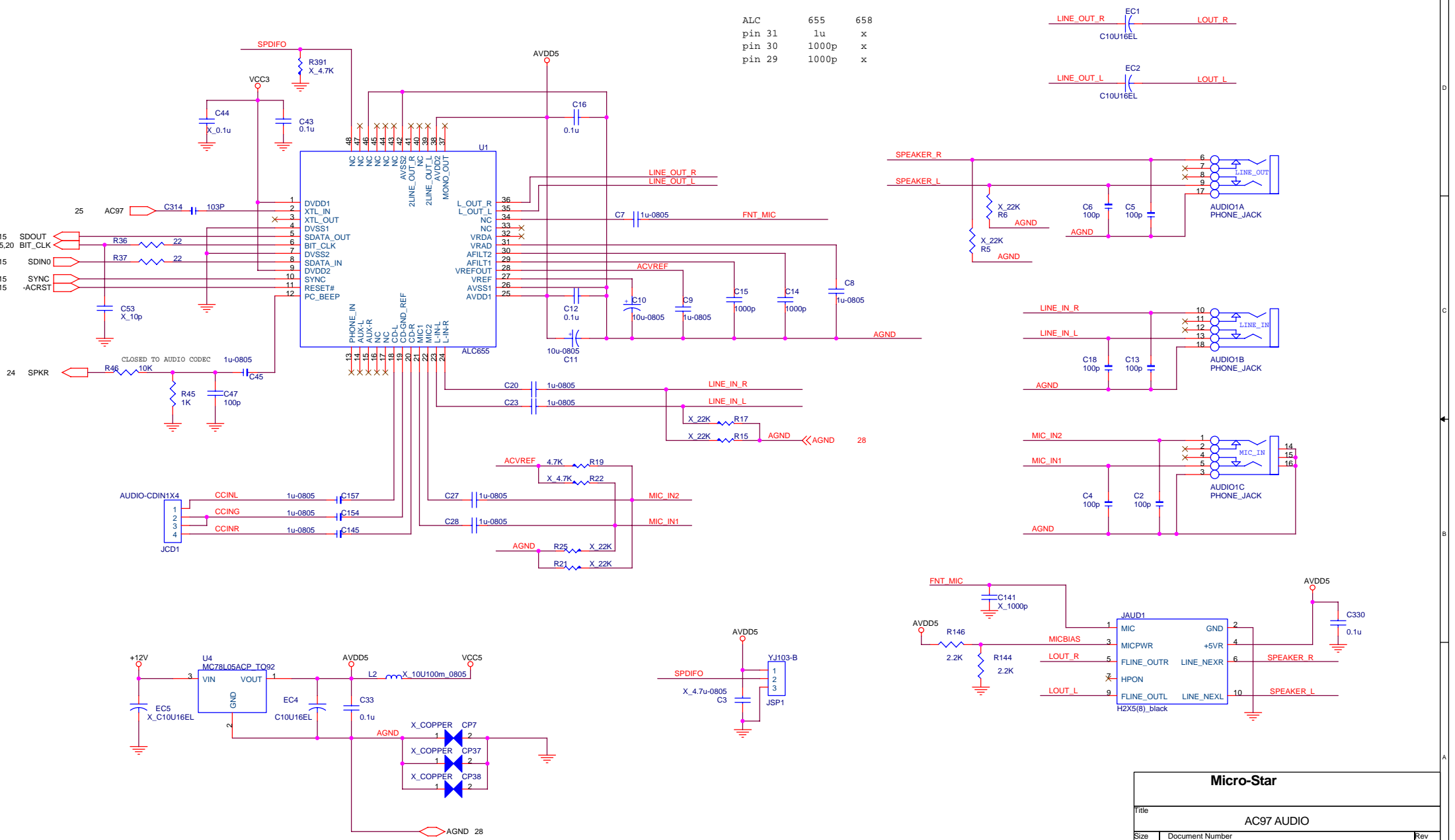
PCI SLOT DECOUPLING CAPACITORS



Micro-Star

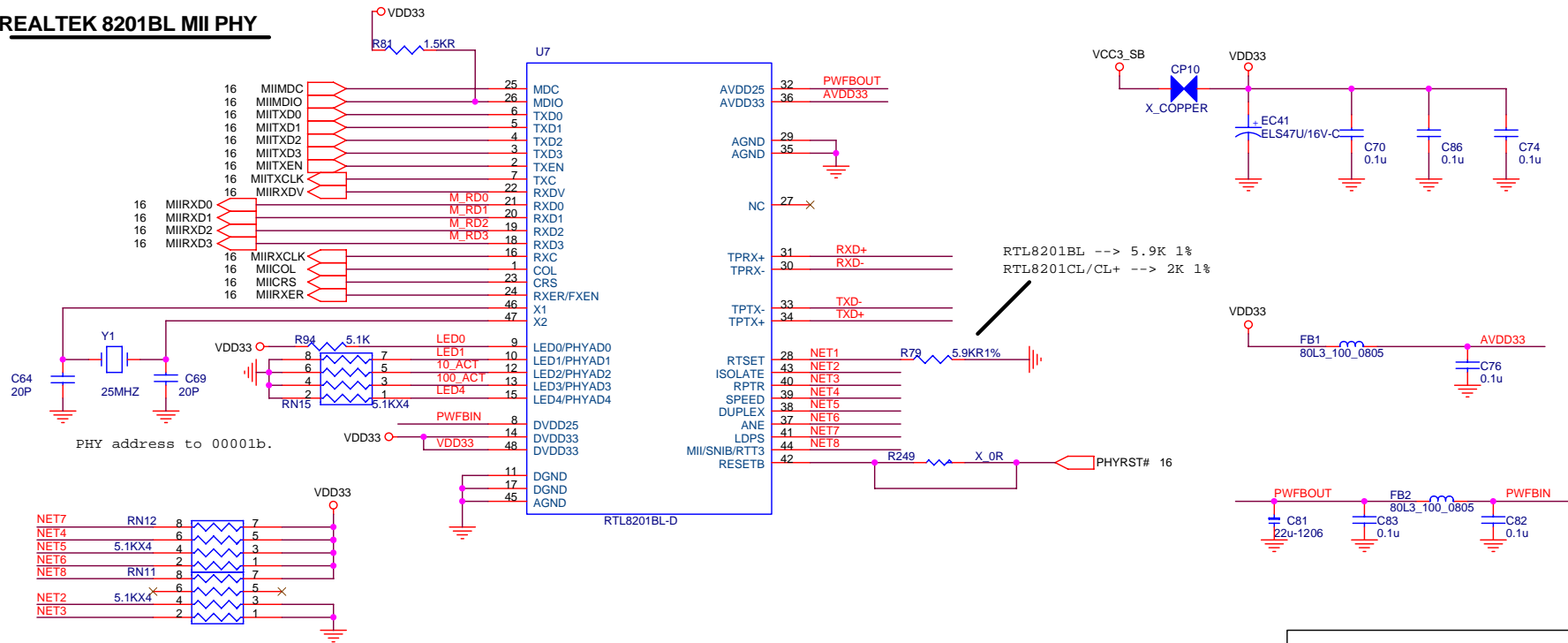
Title			PCI 1 & 2 & 3 Slots	
Size	Document Number		MS-7004	Rev 10A
Date:	Wednesday, February 25, 2004	Sheet	17	of 29

ALC	655	658
pin 31	1u	x
pin 30	1000p	x
pin 29	1000p	x



Micro-Star			
Title			
AC97 AUDIO			
Size	Document Number		Rev
	MS-7004		10A
Date:	Wednesday, February 25, 2004	Sheet	18 of 29

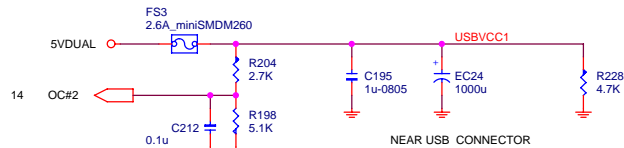
REALTEK 8201BL MII PHY



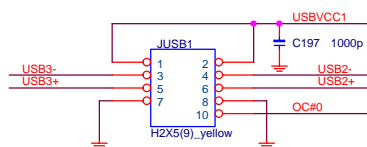
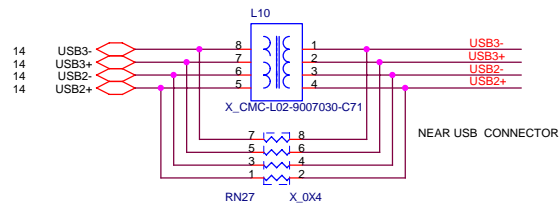
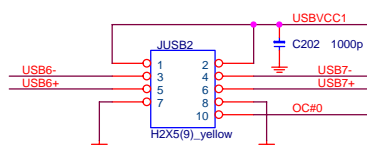
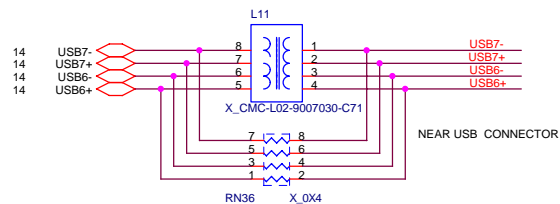
Micro-Star

Title			DLED BRACKET
Size	Document Number		Rev
	MS-7004		10A
Date:	Wednesday, February 25, 2004	Sheet	19 of 29

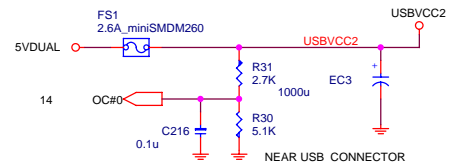
POWER CIRCUIT FOR USB PORT 4,5,6,7



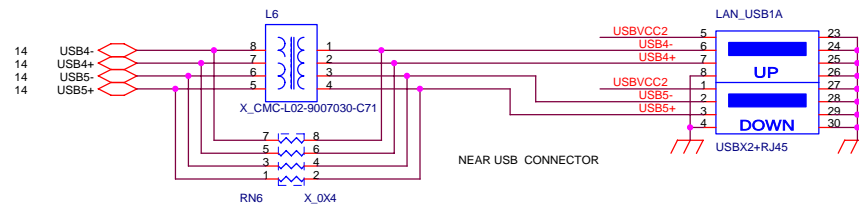
REAR PANEL USB CONNECTOR FOR USB PORT 4,5,6,7



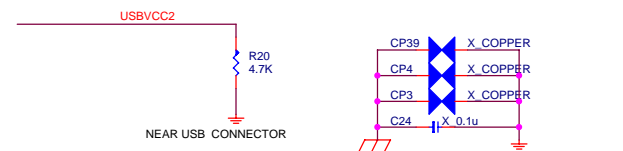
POWER CIRCUIT FOR USB PORT 2,3



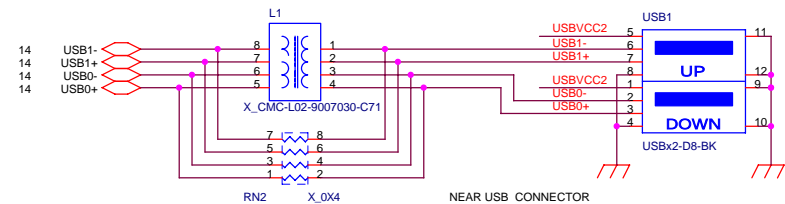
REAR PANEL USB CONNECTOR FOR USB PORT 2,3



POWER CIRCUIT FOR USB PORT 0,1



REAR PANEL USB CONNECTOR FOR USB PORT 0,1

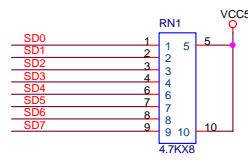
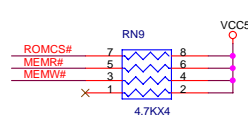


Micro-Star

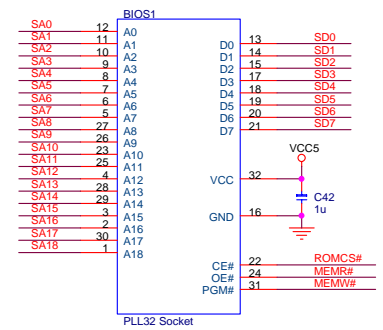
Title		
USB Connectors		
Size	Document Number	Rev
	MS-7004	10A
Date:	Wednesday, February 25, 2004	Sheet 21 of 29

STRAPS

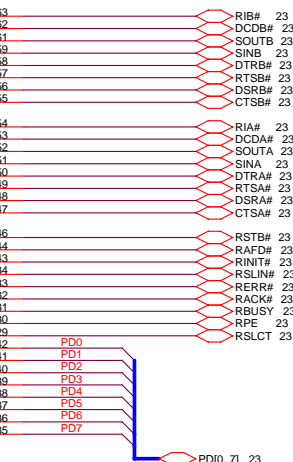
RTSA#	L: CFAD=2E	H: CFAD=4E
SOUTB	L: 24MHZ	H: 48MHZ



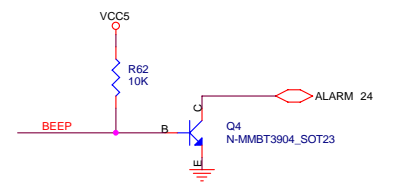
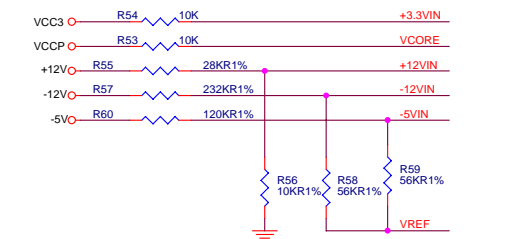
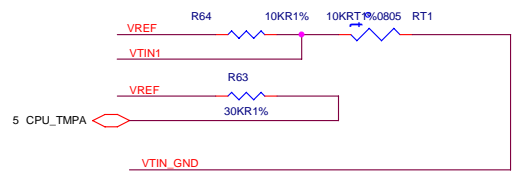
Flash Rom



W83697HF

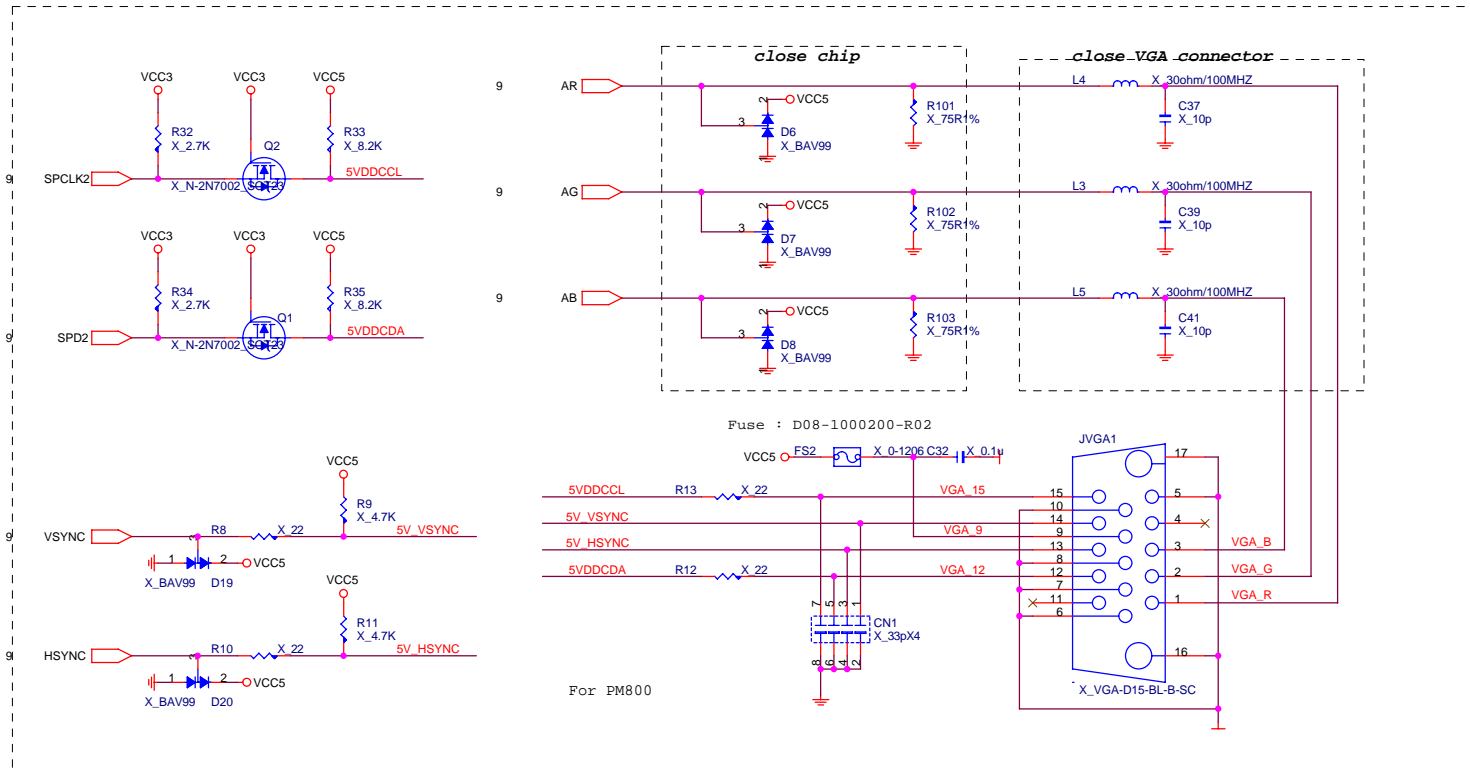
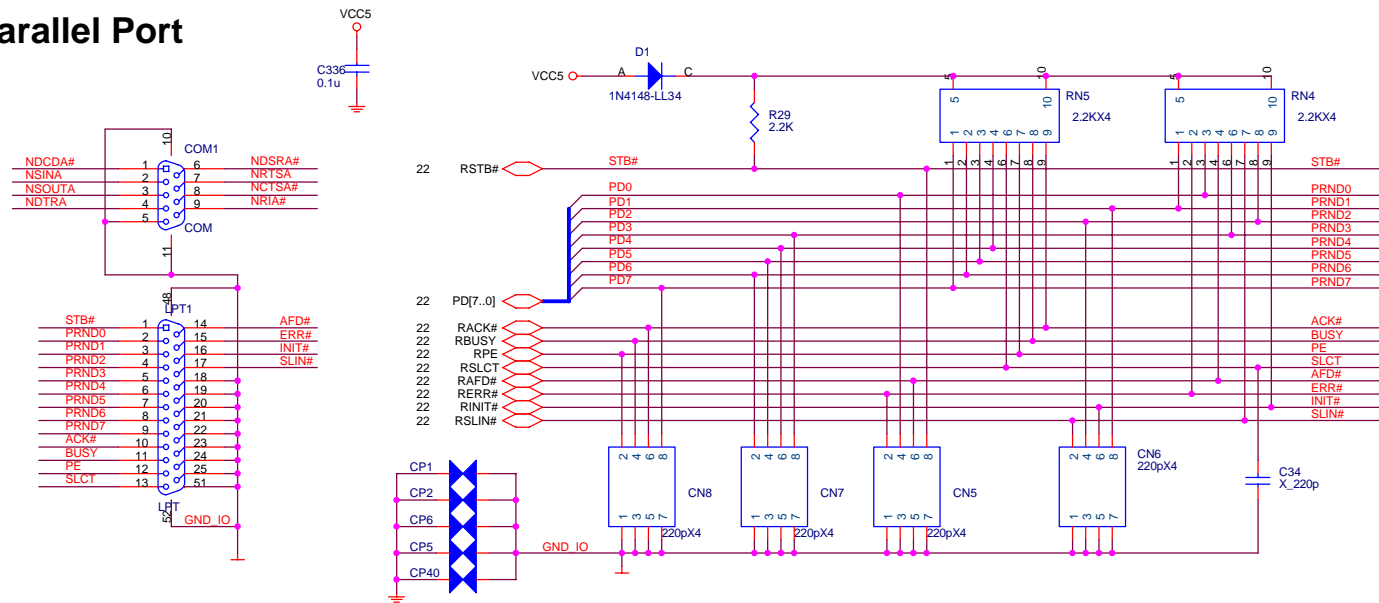


Hardware Monitor

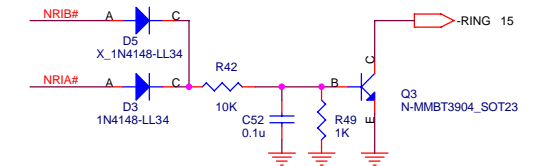
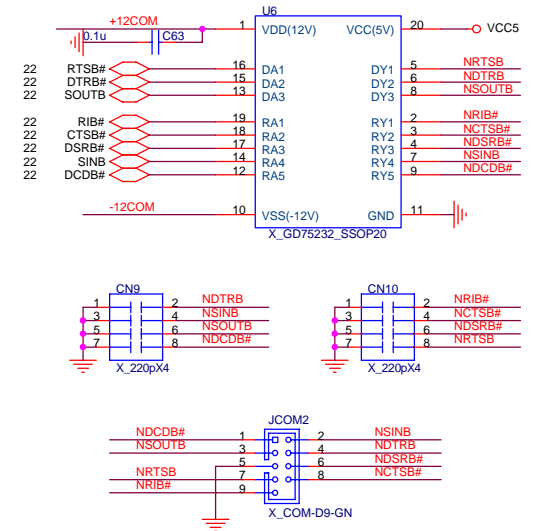
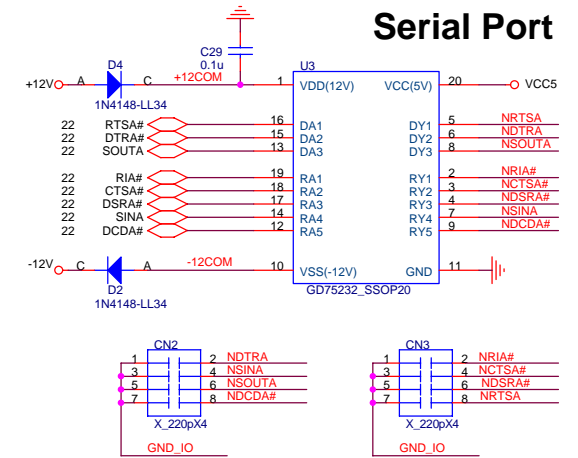


Micro-Star		
Title		
LPC I/O(W83697HF)		
Size	Document Number	Rev
MS-7004		10A
Date:	Wednesday, February 25, 2004	Sheet 22 of 29

Parallel Port

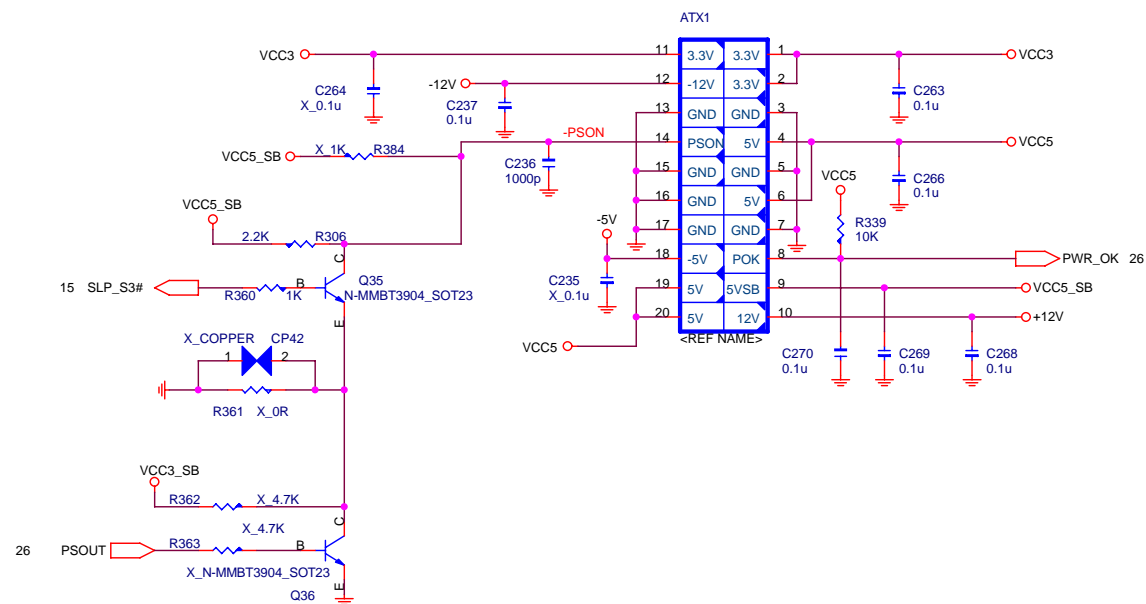


Serial Port

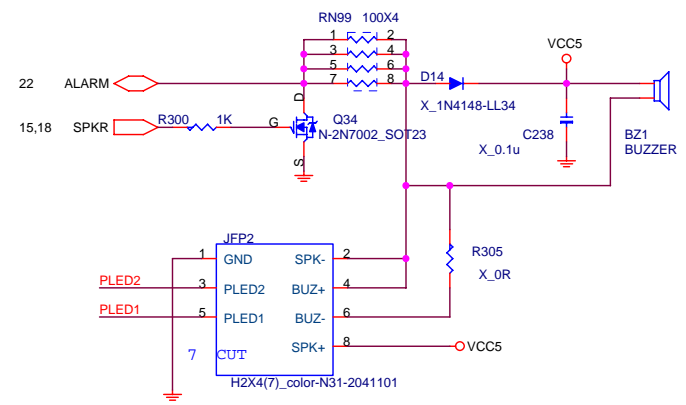


Micro-Star			
Title			
Parallel/Serial Port			
Size	Document Number	Rev	
MS-7004		10A	
Date:	Wednesday, February 25, 2004	Sheet	23 of 29

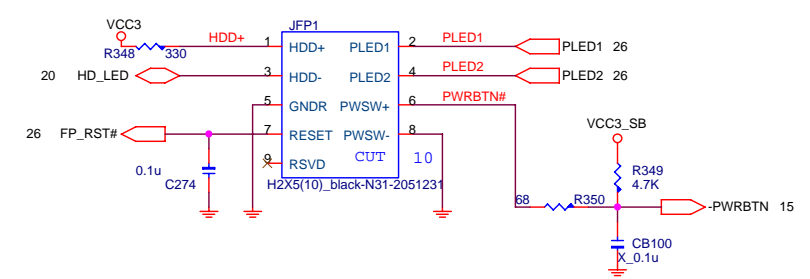
ATX Connector



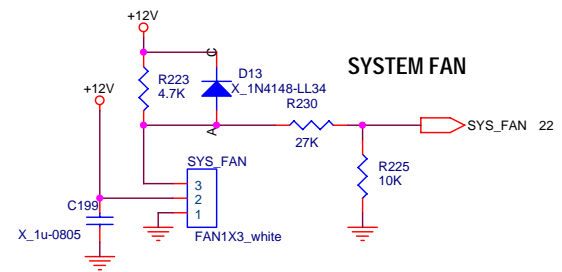
MSI Front Panel Connector



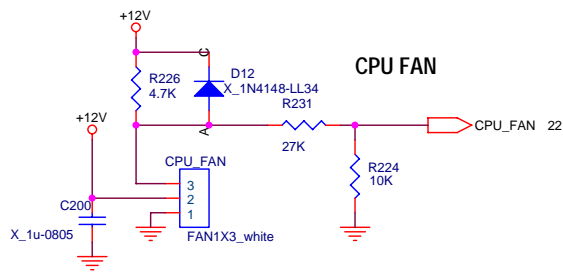
INTEL/PB Front Panel Connector



SYSTEM FAN

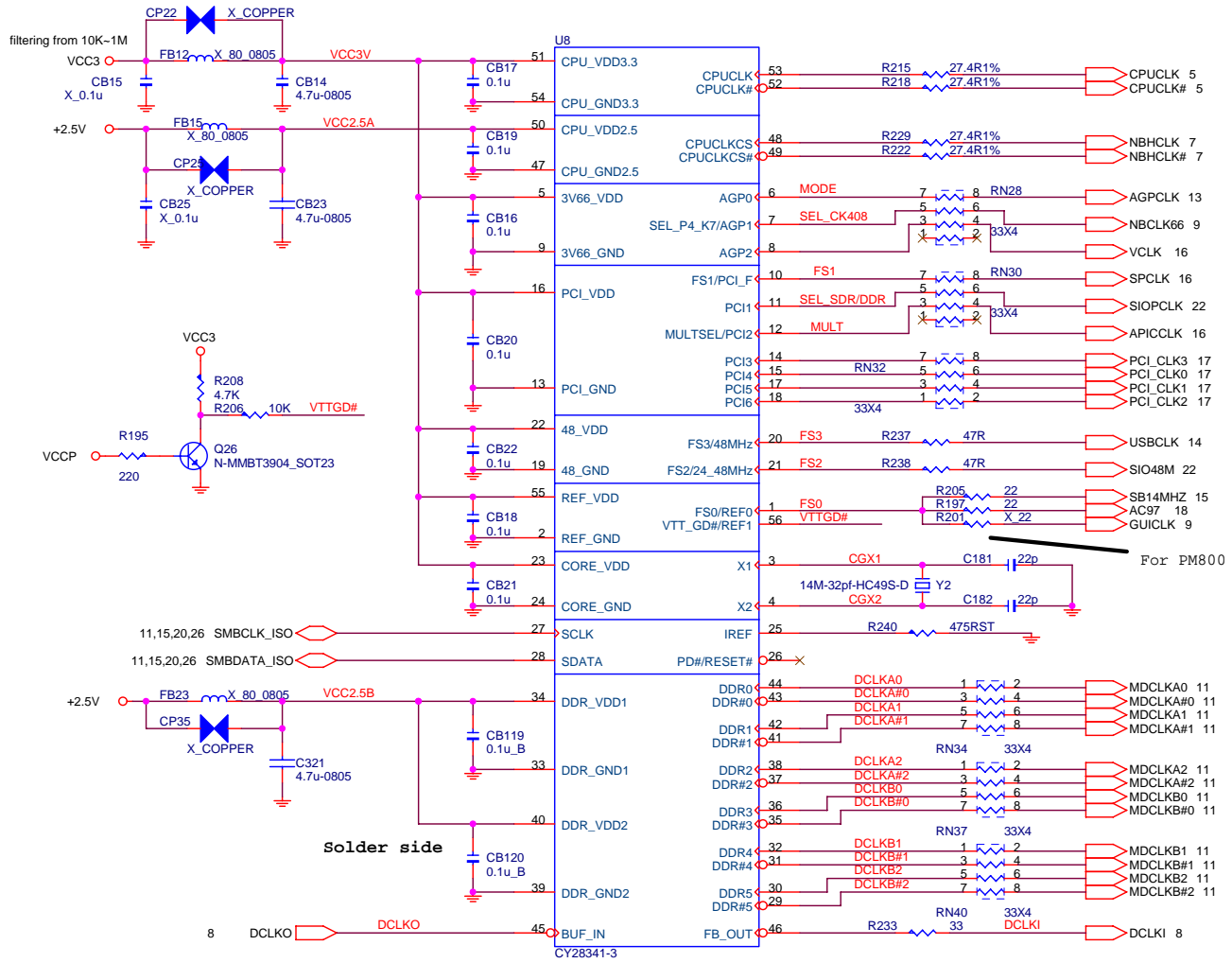


CPU FAN

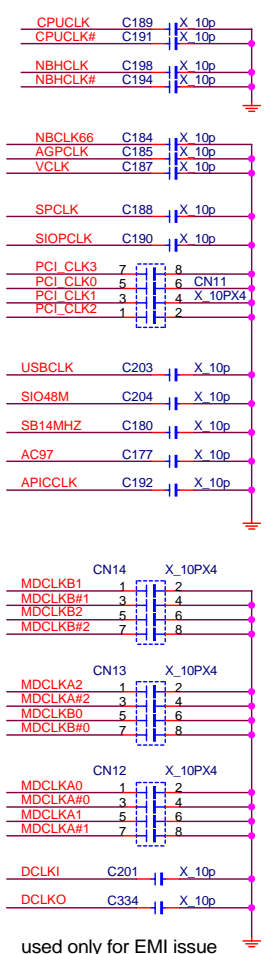


Micro-Star

Title					
ATX Connector & Front Panel					
Size	Document Number				Rev
MS-7004				10A	
Date:	Wednesday, February 25, 2004			Sheet	24 of 29
2		1			



Pull-Down Capacitors



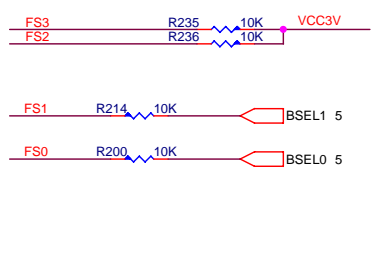
used only for EMI issue
Trace less 0.2"

Shut Source Termination Resistors

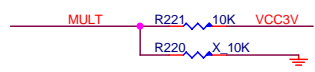
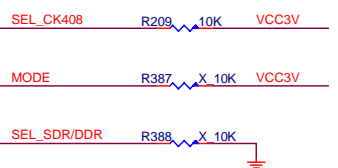


Trace less 0.2" 49.9ohm for 50ohm M/B impedance

CLOCK STRAPPING RESISTORS



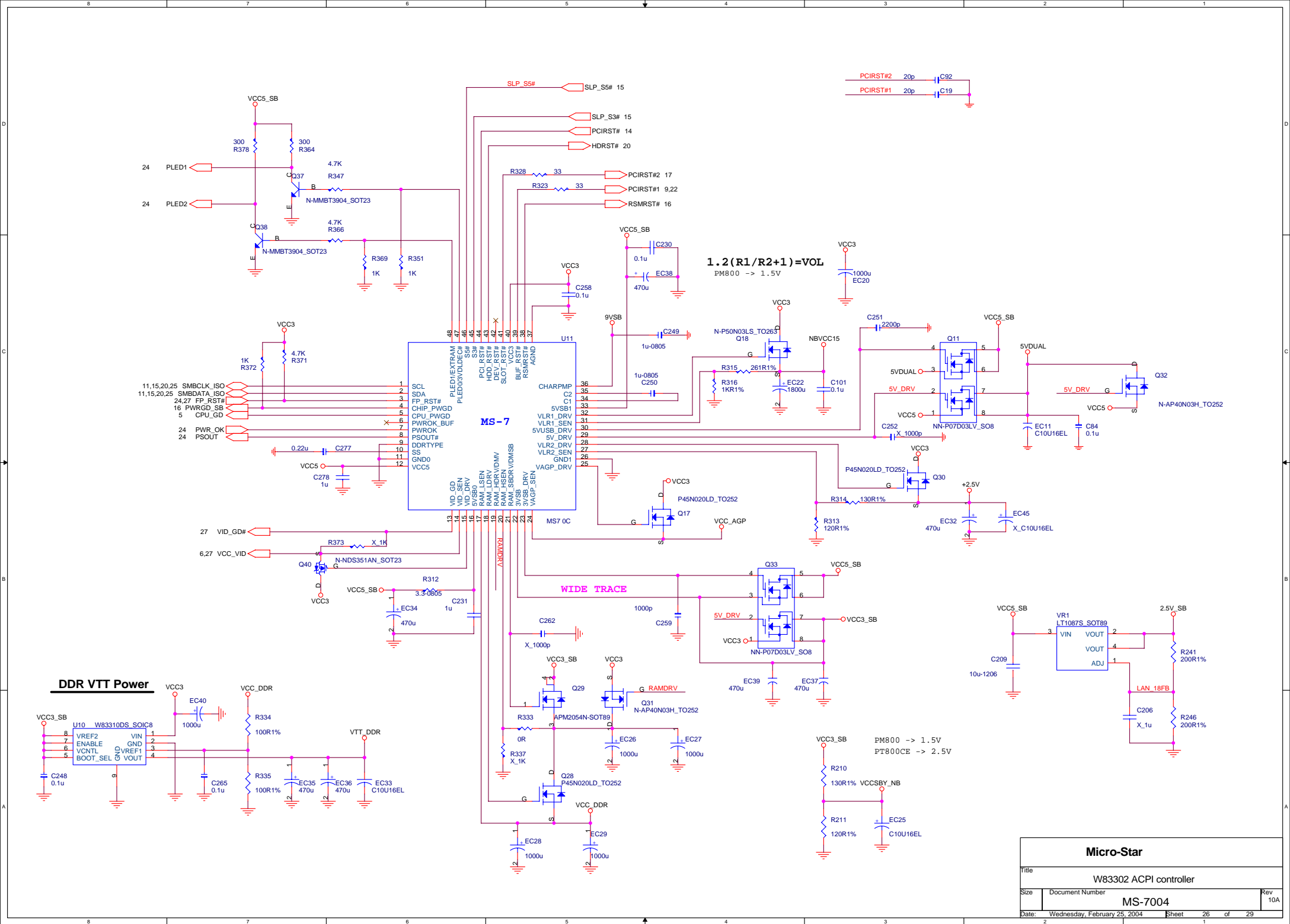
FS3	FS2	FS1	FS0	FSB (MHz)
1	1	0	0	100 MHz
1	1	0	1	133 MHz
1	1	1	0	200 MHz
1	1	1	1	166 MHz



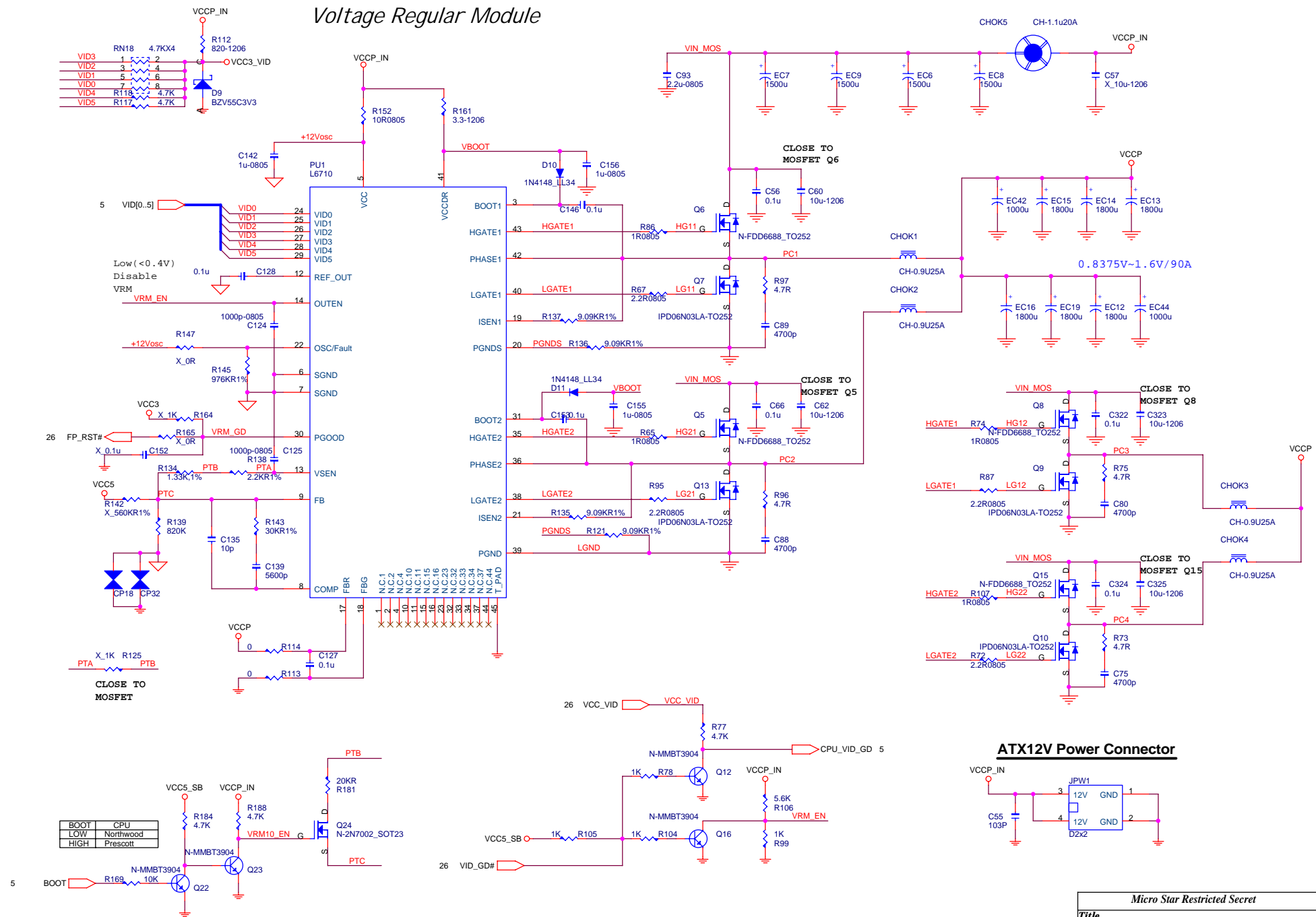
MULT	Rr	Iref	Ioh	Voh
0	221	5.00mA	4*Iref	1.0V
1	475	2.32mA	6*Iref	0.7V

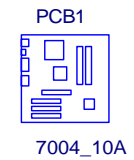
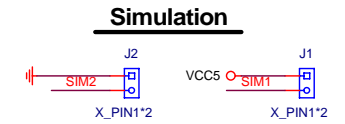
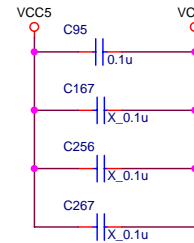
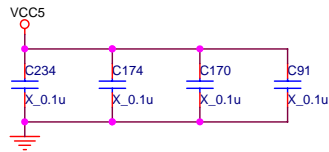
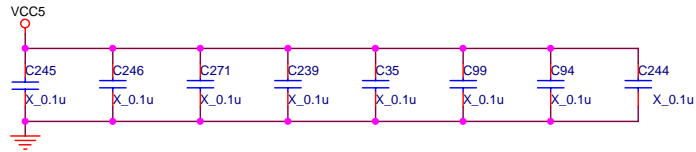
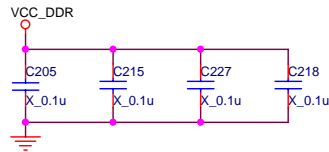
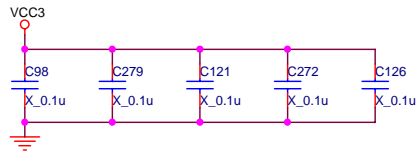
Micro-Star

Clock Generator



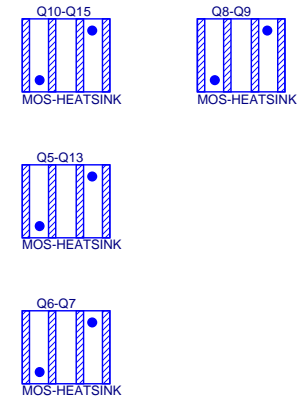
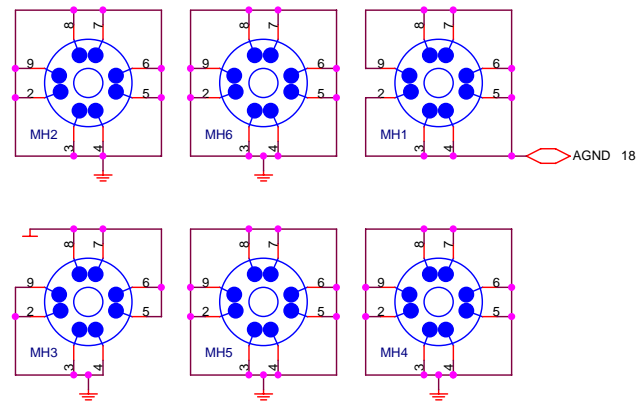
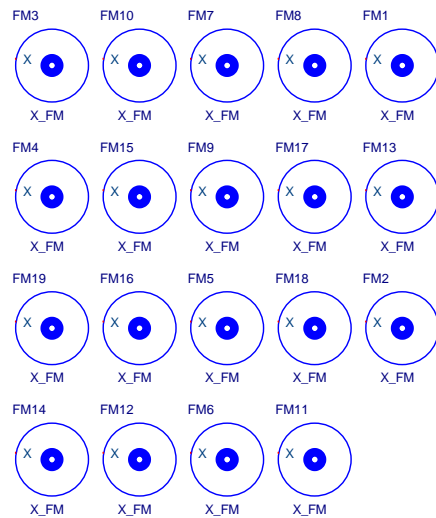
Voltage Regular Module





Mounting Holes

Optics Orientation Holes



Micro-Star

Title				EMI PART
Size	Document Number			MS-7004
Date:	Wednesday, February 25, 2004	Sheet	28 of 29	Rev 10A

MS-7004 VOC	
1.	北橋ballout change to PM800/PT800 VER:B , Add 電源Pin .
2.	Modify PWM layout & placemant .
3.	Modify CPU & CHIPS 電源VCCP.NBVCC15內層切割.
4.	Delete 預留VT8235CE的電阻.
5.	Delete U5(Transform),改用有包進去的Lan connector .
6.	BIOS ROM 與 FANCPU1 卡機構問題 & CPUFAN 與 SYSFAN 互換
7.	Modify NB VCCDAC & VCCPLL 線路.
8.	NB 電源背焊電容改成10u/0805.
9.	Modify U8(Clock Generator)電源線路,Add ICS strapping resistors.
10.	加粗VCC5_SB & VCC3_SB切內層

MS-7004 V100	
1.	Modify net VID_GD# circuit
2.	Change some resistors & cap for VRM transient.
3.	加寬 net CPU_TMPA(CPU to I/O) & VCCP_IN(JPW1 to PU1)
4.	Modify VRM layout
5.	ADD NB pin Y6,AB5,AB6 pull down resistors & pin N3接地
6.	DDR BUS 0 ohm 直接短路
7.	C92,C19移至U11端,ADD C334 for net DCLKO
8.	Bios Rom VCC5 trace 拉至C42
9.	R389,R390,R249,R361 直接短路,cost down 0 ohm
10.	USB 0 ohm 排阻直接短路
11.	Modify VCC5 Plane for IDE BUS 跨切割
12.	VCC5 trace 拉粗至12~25 mils
13.	Modify net CPU_GD & VCC_VID & VCC_AGP_SEN & VTIN_GND 走線

MS-7004 V10A	
1.	ADD IDE 排阻
2.	Modify LAN 10/100 燈號線路
3.	Modify VRM 切割
4.	Delete JSLP1
5.	Modify +2.5V 切割區 & USB 5VDAUL 切割區
6.	change USB Rset >>> 5.9K & VGA Rset >>> 82 ohm
7.	ADD C335 20P for 北橋 PCIRST#1
8.	LVREF_SB >>> 0.3V (R276 >>> 412ohm)

Micro-Star		
Title History 1		
Size	Document Number	Rev 10A
MS-7004		
Date:	Wednesday, February 25, 2004	Sheet 29 of 29